

PRIOR ART

FIG. 1

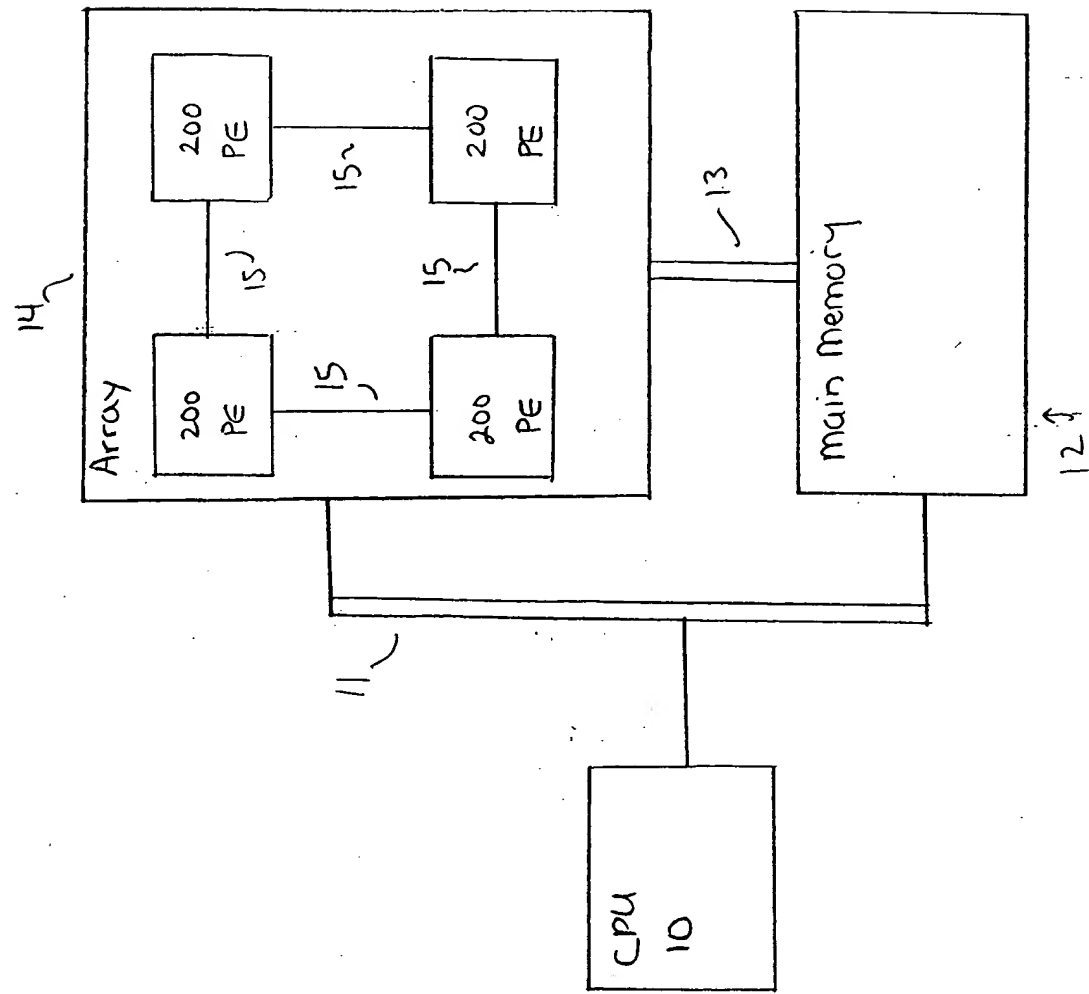


FIG. 2

FIG 300

Q-Block 350b

M-Block 350a

Q-Bus 307b

M-Bus 307a

307a

309a

308a

330

Q3

331

Q2

332

Q1

333

Q0

334

QS

309b

320

G

310

M3

311

M2

312

M1

313

M0

314

MS

REGISTER  
FILE

302

ALU

301

Node  
Communications  
Interface

305

306a

306b

306c

306d

307

FLAGS

SHIFT CONTROL  
REGISTER

308

DRAM  
Interface

303

304

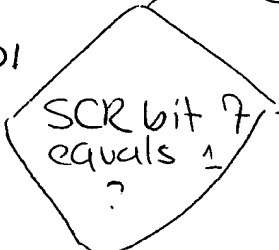
FIG 3

FIG 4A

START

400

401



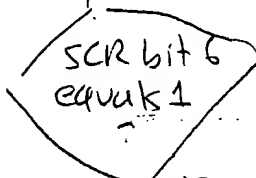
Yes

402

Set M2=0, M1=0, M0=0

No

403



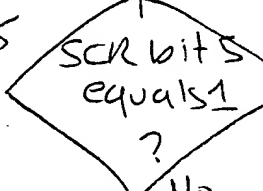
Yes

404

Set M2=0, M1=0, M0=0

No

405



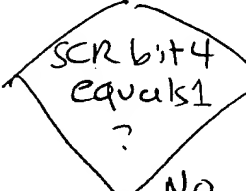
Yes

406

Set M2=0, M1=0, M0=0

No

407



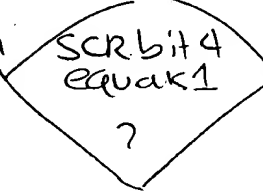
Yes

408

Right shift by 8-bits  
M2, M1, M0

No

409



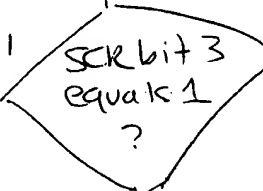
Yes

410

Right Shift by 8-bits  
M2, M1, M0

No

411



Yes

412

Right Shift by 8-bits  
M2, M1, M0

A

FIG 4B

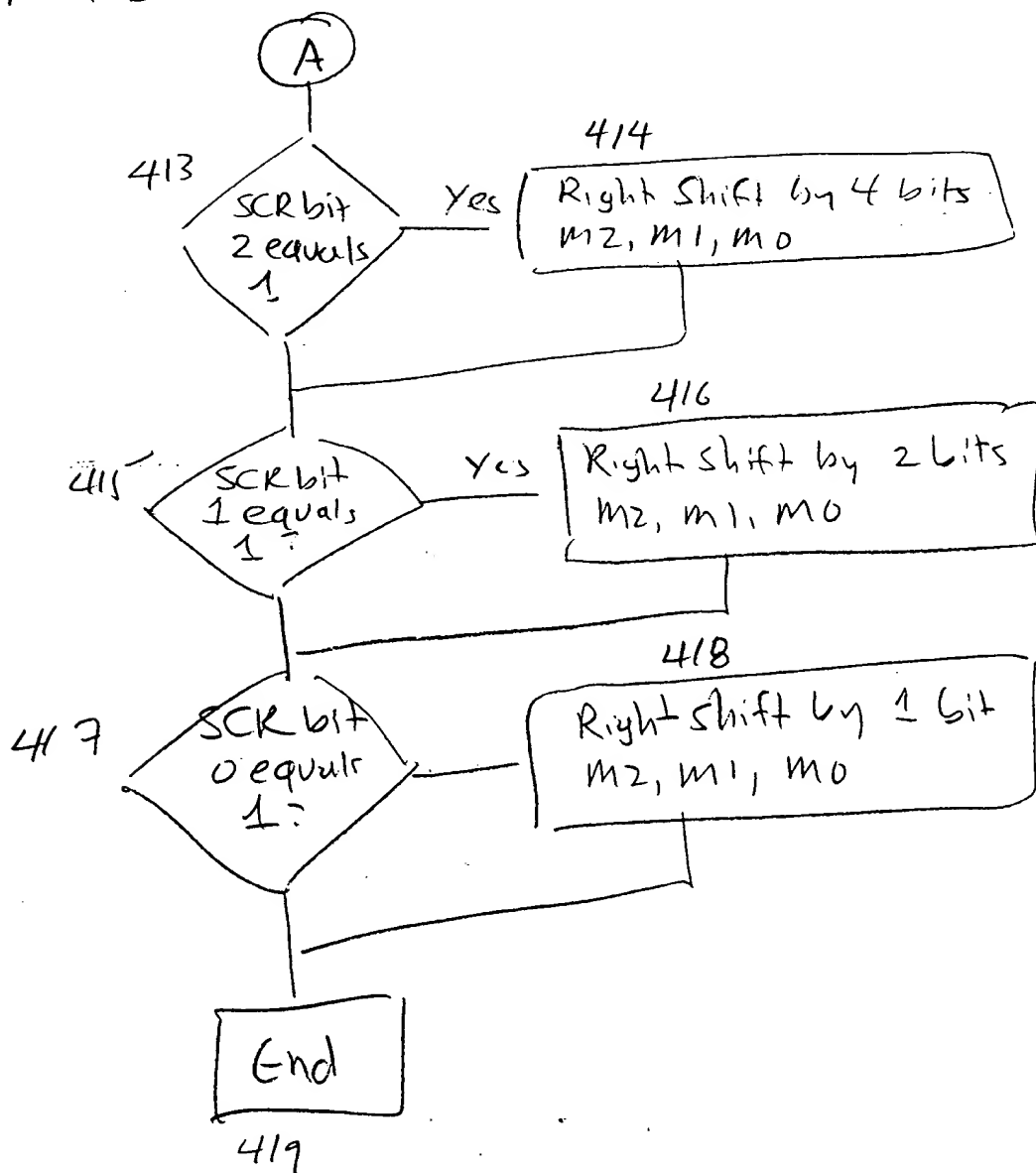


FIG 5

